works well with load impedances of at least 2 kΩ. At impedances higher than that value, parasitic impedances associated with the terminating resistor and IC_1 degrade bandwidth and pulse fidelity.

In a back-terminated, 50Ω system, the circuit delivers a 4.5V output pulse with symmetric rise and fall times of 1.5 nsec, pulse-top-amplitude aberrations of less than 10%, and amplitude droop of less than 5%. Directly driving a 50Ω load doesn't degrade the output's rise and fall times. For best pulse fidelity, use stripline techniques to route IC_1's output directly to the termination resistor and output connector J_1. Using a 100-mil-wide trace on a 1/16-in., double-sided, glass-epoxy pc board approximates a 50Ω surge impedance. EDN

Shift registers and resistors deliver multiphase sine waves

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Sine waves with fixed phase relationships find application in communications equipment, instrumentation, and power sources. Although you can use any of several traditional analog techniques to generate basic sine-wave signals, this Design Idea offers a simple method that uses only digital logic and fixed-value resistors (**Figure 1a**). A common clock pulse drives three of four sections of a pair of CD4015 4-bit shift registers that recirculate a pattern comprising 12 zeros and 12 ones—that is, 000000000000-011111111111. Each of the registers' outputs drives a resistor, R_1 through R_{12}, that connects to a summing node. If all of the resistors were of equal value, their summed output would comprise a stepped linear triangular waveform at a repetition frequency one-twenty-fourth that of the clock frequency.

To produce a stepped sinusoidal output waveform, you replace the equal-value resistors with the weighted values in **Figure 1a**. If you use resistors of 1% tolerance, the output's amplitude will approximate that of a true sine wave to better than 1°. To produce a cleaner sine wave, a lowpass filter helps remove clock-pulse feedthrough and stepped-edge transients (**Figure 1b**). For many applications, a simple one-pole lowpass filter/buffer provides adequate filtering, but a more elaborate multipole filter further increases output purity.

You can add a second set of registers and resistors, R_{13} through R_{24}, to produce cosine and sine waves offset by a 90° phase shift—that is, two sine waves in quadrature (**Figure 2**). Register IC_{2A}'s inverted and recirculated output from Q4 generates the 0000000000-00111111111111 bit pattern that the first set of shift registers uses. IC_{2B}'s Q4 output produces the D input that you apply to the second set of shift registers—IC_{2B}, IC_{3A}, and IC_{3B}—which in turn generate a 90° phase-shifted version of the bit pattern to form a cosine wave. The cosine bit pattern requires no recirculation and simply propagates

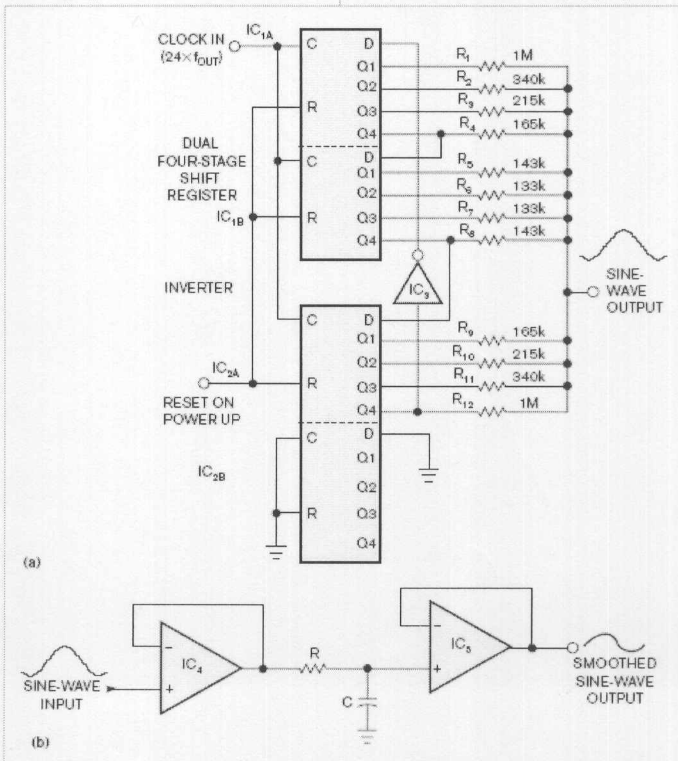

Figure 1 A pair of shift registers, an inverter, and a handful of precision resistors form a sine-wave generator (a). Two operational amplifiers form a resistance-capacitance lowpass filter that removes clock-signal artifacts from the output (b).

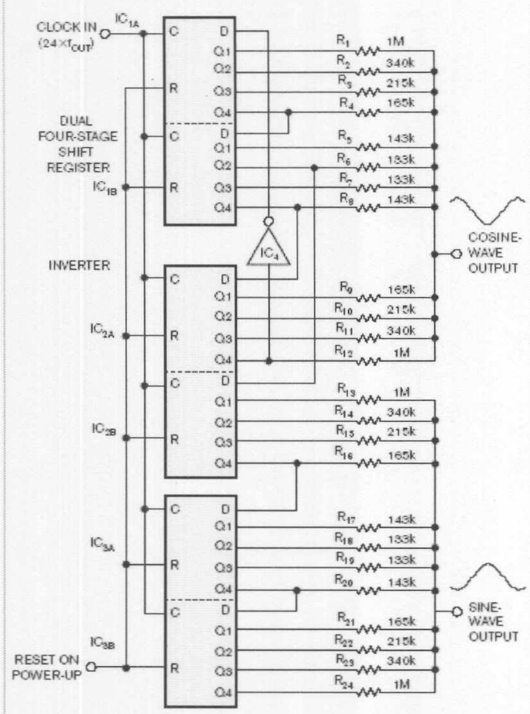

Figure 2 Add a second set of shift registers to generate a cosine wave.

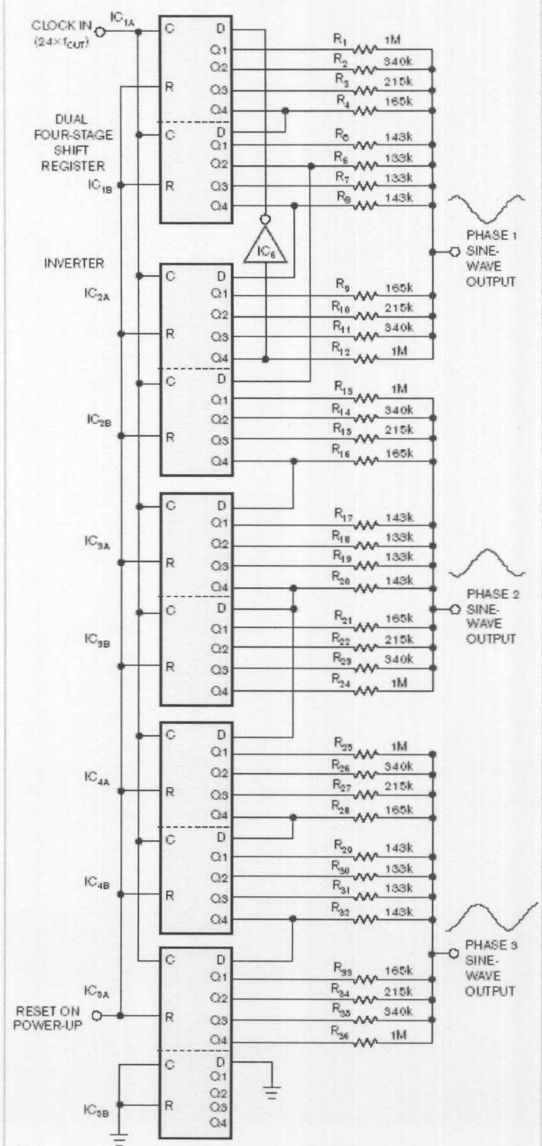

Figure 3 Adding a third set of shift registers yields a three-phase sine-wave output.

through the second set of shift registers and "falls off the end." To adjust the second output's phase shift with respect to the first output from 15 to 180° in 15° increments, you can connect IC_{2A}'s D input to any one of IC_1's Q outputs.

Figure 3 illustrates a three-phase sine-wave-generator circuit. The Q4 output from IC_{1B} supplies the D input to the second set of shift registers, IC_{2A} and IC_{2B}, to produce the recirculated bit pattern. In similar fashion, the Q4 output from IC_{3A} supplies the D input to the third set of shift registers, IC_{4A}, to transfer a duplicate bit pattern that's phase-shifted by 240° with respect to the output from the first set of shift registers.

Register IC_{2B}'s D input connects to IC_{1B}'s Q4 output to produce a signal—Phase 2's output—that lags behind the Phase 1 output by 120°. In similar fashion, register IC_{4A}'s D input connects to IC_{3A}'s Q4 output to produce a signal—Phase 3's output—that lags behind Phase 2's output by 120°, or 240° with respect to Phase 1.

You can expand the basic circuit to accommodate additional signal phases. The weighted resistors' values are adequate for low-frequency sine waves and 4000-series CMOS-logic devices. However, you can scale the resistors' values to accommodate other output frequencies and logic families. EDN